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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/610,478	06/30/2003	Shekoufeh Qawami	ITL.1031US (P16767)	9348

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EXAMINER	
BATAILLE, PIERRE MICHE	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/610,478	QAWAMI ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/06/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-17 and 22-25 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,784,331 (Lysinger).

With respect to claim 1 and 22, Lysinger discloses a method, comprising: sensing a first word group from a first address of a memory while sensing a second word group from a second address of the memory ***[(read cycle divided in two parts and in parallel, a first part accessing address memory cells at a faster burst count Col. 19, Lines 52-57) while data is burst counted out of the memory device at the rate defined, access at another random location is occurring in parallel, Col. 20, Lines 9-13; Col. 4, Lines 15-27)].***

With respect to claim 8, Lysinger discloses sensing a first burst length of data equal to half of a sense width of a plurality of sense amplifiers of a memory ***[(sense amplifiers located in the block I/O circuitry for accessing a memory cell in the memory array 52) Col. 19, Lines 52-57; Col. 16, Line 62 to Col. 17, Line 28]***; and sensing a second burst length of data equal to the half of the sense width at least partially during a latency before reading the first burst length

of data [***while data is burst counted out of the memory device at the rate defined, access at another random location is occurring in parallel, Col. 20, Lines 9-13); Col. 17, Lines 5-38]***.

With respect to claim 11, Lysinger discloses sensing a third burst length of data equal to the half of the sense width after sensing the first burst length ***[Fig. 11; Col. 7, Line 56 to Col. 8, Line 2 (while data is burst counted out of the memory device at the rate defined, access at another random location is occurring in parallel, Col. 20, Lines 9-13); Col. 17, Lines 5-38]***.

With respect to claim 12, Lysinger discloses a method, comprising: sensing a first word group from a first address of a memory while sensing a second word group from a second address of the memory, a first latch to the first address and a second latch to the first address ***[Fig. 10 and 12; (read cycle divided in two parts and in parallel, a first part accessing address memory cells at a faster burst count Col. 19, Lines 52-57) while data is burst counted out of the memory device at the rate defined, access at another random location is occurring in parallel, Col. 20, Lines 9-13); Col. 17, Lines 5-38].***

With respect to claim 2, 14, and 23, Lysinger discloses the method, wherein the first word is half as wide as a sense width of a sense array of group the memory ***[Col. 19, Lines 52-57; Col. 16, Line 62 to Col. 17, Line 28***].

With respect to claims 3 and 9, Lysinger discloses the method synchronously reading the first word group and the second word group from the memory ***[time sequences under control of burst counter and clock cycles (Col. 18, Line 38-61)].***

With respect to claim 4 and 24, Lysinger discloses separating a request for the first word group from a request for the second word group by a predetermined number of clock cycles ***[a new burst started just prior to final selection stage, a new address is provided at any convenient time during time interval of the first read Col. 18, Lines 38-54].***

With respect to claim 5, Lysinger discloses the predetermined number equal to four ***[timing sequences of predetermined number (Fig. 9B; Col. 18, Lines 38-54; Col. 16, Line 62 to Col. 17, Line 28)]***.

With respect to claims 6 and 10, Lysinger discloses words of variable size wherein the first word group comprises four double words ***[Fig. 9B; Col. 16, Line 62 to Col. 17, Line 28]***.

With respect to claim 7, Lysinger discloses using a first latch to the first address and a second latch to the first address ***[Fig. 10 and 12; Col. 17, Lines 5-38].***

With respect to claim 13, Lysinger discloses a first latency counter to track the latency of the first read operation ***[Col. 17, Lines 3-35]***.

With respect to claims 15-17, Lysinger discloses array to sense information in a first read operation and a second read operation, sensing of

information are from a single initial address or a non-contiguous address of the memory ***[Fig. 1-2, and 10; Col. 4, Lines 47-63]***.

With respect to claim 25, Lysinger discloses enabling the system to sense a third word group while the first word group is read ***[while data is burst counted out of the memory device at the rate defined, access at another random location is occurring in parallel, Col. 20, Lines 9-13].***

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,784,331 (Lysinger et al).

With respect to claim 18, Lysinger discloses a memory having a sense array to overlappingly sense a first word from a first address and a second word from a second address ***(while data is burst counted out of the memory device at the rate defined, access at another random location is occurring in parallel, Col. 20, Lines 9-13); Col. 17, Lines 5-38]***. Lysinger fails to specifically teach a dipole antenna coupled to the memory. However, such is not novel in the field of the art as, it is known to have connected memory with a dipole antenna to make use of the dipole high frequency to transmit information stored in the memory section within its semiconductor chip to an external reader-

writer. Therefore, one of ordinary skill in the art would have connect a dipole antenna to the memory to make use of the dipole high frequency to transmit information stored in the memory section within its semiconductor chip to an external reader-writer. A dipole antenna is operative to transmit radio frequency signals (RF) from integrated circuit chip to a controller and to receive incoming RF signals from an external RF source controller.

With respect to claims 19-21, Lysinger discloses a first latency counter to track a latency associated with a read operation, the sense array having a width twice the first word group, a first output buffer coupled to the first portion of the sense array ***[Col. 4, Lines 28-42].***

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6914830 (Merritt) teaching distributed write data drivers for burst access memories.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon-Fri (8:00A to 4:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

December 9, 2005

PIERRE BATAILLE
PRIMARY EXAMINER